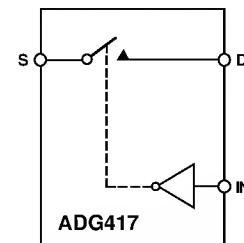


FEATURES

44 V Supply Maximum Ratings
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (<35 Ω)
Ultralow Power Dissipation (<35 μ W)
Fast Switching Times
 t_{ON} (145 ns max)
 t_{OFF} (100 ns max)
Break-Before-Make Switching Action
Latch-Up Proof
Plug-In Replacement for DG417

APPLICATIONS

Precision Test Equipment
Precision Instrumentation
Battery Powered Systems
Sample Hold Systems

FUNCTIONAL BLOCK DIAGRAM

 SWITCH SHOWN FOR A
 LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG417 is a monolithic CMOS SPST switch. This switch is designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents. Trench isolation gives all the benefits of dielectric isolation and ensures no latch-up even under extreme overvoltage conditions.

The on resistance profile of the ADG417 is very flat over the full analog input range ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG417 switch, which is turned ON with a logic low on the control input, conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG417 exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital input.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
 The ADG417 is fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range that extends to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch-Up
 A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions
5. Single Supply Operation
 For applications where the analog signal is unipolar, the ADG417 can be operated from a single rail power supply. The part is fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

REV. 0

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ADG417—SPECIFICATIONS¹

Dual Supply ($V_{DD} = +15 \text{ V} \pm 10\%$, $V_{SS} = -15 \text{ V} \pm 10\%$, $V_L = +5 \text{ V} \pm 10\%$, $GND = 0 \text{ V}$, unless otherwise noted)

Parameter	B Version +25°C -40°C to +85°C		T Version +25°C -55°C to +125°C		Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range	V _{SS} to V _{DD}		V _{SS} to V _{DD}		V	
R _{ON}	25	45	25	45	Ω typ	V _D = ±12.5 V, I _S = -10 mA
					Ω max	V _{DD} = +13.5 V, V _{SS} = -13.5 V
LEAKAGE CURRENTS						
Source OFF Leakage I _S (OFF)	±0.1		±0.1		nA typ	V _{DD} = +16.5 V, V _{SS} = -16.5 V
Drain OFF Leakage I _D (OFF)	±0.25	±5	±0.25	±15	nA max	V _D = ±15.5 V, V _S = ±15.5 V;
Channel ON Leakage I _D , I _S (ON)	±0.1		±0.1		nA typ	Test Circuit 2
	±0.25	±5	±0.25	±15	nA max	V _D = ±15.5 V, V _S = ±15.5 V;
	±0.1		±0.1		nA typ	Test Circuit 2
	±0.4	±5	±0.4	±30	nA max	V _S = V _D = ±15.5 V;
						Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V _{INH}	2.4		2.4		V min	
Input Low Voltage, V _{INL}	0.8		0.8		V max	
Input Current					μA typ	
I _{INL} or I _{INH}	±0.005		±0.005		μA max	V _{IN} = V _{INL} or V _{INH}
DYNAMIC CHARACTERISTICS ²						
t _{ON}	100		100		ns typ	R _L = 300 Ω, C _L = 35 pF;
	145	200	145	200	ns max	V _S = ±10 V; Test Circuit 4
t _{OFF}	60		60		ns typ	R _L = 300 Ω, C _L = 35 pF;
	100	150	100	150	ns max	V _S = ±10 V; Test Circuit 4
Charge Injection	7		7		pC typ	V _S = 0 V, R _L = 0 Ω,
OFF Isolation	80		80		dB typ	C _L = 10 nF; Test Circuit 5
C _S (OFF)	6		6		pF typ	R _L = 50 Ω, f = 1 MHz;
C _D (OFF)	6		6		pF typ	Test Circuit 6
C _D , C _S (ON)	55		55		pF typ	
POWER REQUIREMENTS						
I _{DD}	0.0001		0.0001		μA typ	V _{DD} = +16.5 V, V _{SS} = -16.5 V
	1	2.5	1	2.5	μA max	V _{IN} = 0 V or 5 V
I _{SS}	0.0001		0.0001		μA typ	
	1	2.5	1	2.5	μA max	
I _L	0.0001		0.0001		μA typ	
	1	2.5	1	2.5	μA max	V _L = +5.5 V

NOTES

¹Temperature ranges are as follows: B Version: -40°C to +85°C; T Version: -55°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply ($V_{DD} = +12 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $V_L = +5 \text{ V} \pm 10\%$, $GND = 0 \text{ V}$, unless otherwise noted)

Parameter	B Version +25°C to +85°C		T Version +25°C to +125°C		Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range R_{ON}	0 to V_{DD} 40		0 to V_{DD} 40		V Ω typ Ω max	$V_D = +3 \text{ V}$, $+8.5 \text{ V}$, $I_S = -10 \text{ mA}$ $V_{DD} = +10.8 \text{ V}$
LEAKAGE CURRENT						
Source OFF Leakage I_S (OFF)	± 0.1		± 0.1		nA typ	$V_{DD} = +13.2 \text{ V}$
	± 0.25	± 5	± 0.25	± 15	nA max	$V_D = 12.2 \text{ V}/1 \text{ V}$, $V_S = 1 \text{ V}/12.2 \text{ V}$;
Drain OFF Leakage I_D (OFF)	± 0.1		± 0.1		nA typ	Test Circuit 2
	± 0.25	± 5	± 0.25	± 15	nA max	$V_D = 12.2 \text{ V}/1 \text{ V}$, $V_S = 1 \text{ V}/12.2 \text{ V}$;
Channel ON Leakage I_D , I_S (ON)	± 0.1		± 0.1		nA typ	Test Circuit 2
	± 0.4	± 5	± 0.4	± 30	nA max	$V_S = V_D = 12.2 \text{ V}/1 \text{ V}$; Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4		2.4		V min	
Input Low Voltage, V_{INL}	0.8		0.8		V max	
Input Current I_{INL} or I_{INH}	± 0.005 ± 0.5		± 0.005 ± 0.5		μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
DYNAMIC CHARACTERISTICS ²						
t_{ON}	180	250	180	250	ns max	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; $V_S = +8 \text{ V}$; Test Circuit 4
t_{OFF}	85	110	85	110	ns max	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; $V_S = +8 \text{ V}$; Test Circuit 4
Charge Injection	11		11		pC typ	$V_S = 0 \text{ V}$, $R_S = 0 \Omega$, $C_L = 10 \text{ nF}$; Test Circuit 5
OFF Isolation	80		80		dB typ	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$; Test Circuit 6
C_S (OFF)	13		13		pF typ	
C_D (OFF)	13		13		pF typ	
C_D , C_S (ON)	65		65		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.0001		0.0001		μA typ	$V_{DD} = +13.2 \text{ V}$
	1	2.5	1	2.5	μA max	$V_{IN} = 0 \text{ V}$ or 5 V
I_L	0.0001		0.0001		μA typ	$V_L = +5.5 \text{ V}$
	1	2.5	1	2.5	μA max	

NOTES

¹Temperature ranges are as follows: B Version: -40°C to $+85^\circ\text{C}$; T Version: -55°C to $+125^\circ\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Table I. Truth Table

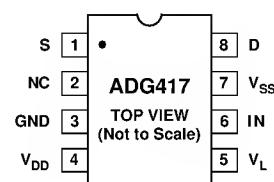
Logic	Switch Condition
0	ON
1	OFF

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG417BN	-40°C to $+85^\circ\text{C}$	N-8
ADG417BR	-40°C to $+85^\circ\text{C}$	SO-8

*N = Plastic DIP, SO = 0.15" Small Outline IC (SOIC).

PIN CONFIGURATION DIP/SOIC



ADG417

ABSOLUTE MAXIMUM RATINGS¹

($T_A = +25^\circ\text{C}$ unless otherwise noted)

V _{DD} to V _{SS}	+44 V
V _{DD} to GND	-0.3 V to +25 V
V _{SS} to GND	+0.3 V to -25 V
V _L to GND	-0.3 V to V _{DD} + 0.3 V
Analog, Digital Inputs ²	V _{SS} - 2 V to V _{DD} + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Extended (T Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C

Plastic Package, Power Dissipation	400 mW
θ_{JA} , Thermal Impedance	100°C/W
Lead Temperature, Soldering (10 sec)	+260°C
SOIC Package, Power Dissipation	400 mW
θ_{JA} , Thermal Impedance	155°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

V _{DD}	Most positive power supply potential.	V _D (V _S)	Analog voltage on terminals D, S.
V _{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.	C _S (OFF)	"OFF" switch source capacitance.
V _L	Logic power supply (+5 V).	C _D (OFF)	"OFF" switch drain capacitance.
GND	Ground (0 V) reference.	C _D , C _S (ON)	"ON" switch capacitance.
S	Source terminal. May be an input or an output.	t _{ON}	Delay between applying the digital control input and the output switching on.
D	Drain terminal. May be an input or an output.	t _{OFF}	Delay between applying the digital control input and the output switching off.
IN	Logic control input.	V _{INL}	Maximum input voltage for logic "0."
R _{ON}	Ohmic resistance between D and S.	V _{INH}	Minimum input voltage for logic "1."
I _S (OFF)	Source leakage current with the switch "OFF."	I _{INL} (I _{INH})	Input current of the digital input.
I _D (OFF)	Drain leakage current with the switch "OFF."	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I _D , I _S (ON)	Channel leakage current with the switch "ON."	Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
		I _{DD}	Positive supply current.
		I _{SS}	Negative supply current.
		I _L	Logic supply current.

TRENCH ISOLATION

In the ADG417, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of the CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.

Trench isolation also leads to lower leakage currents. The ADG417 has a leakage current of 0.25 nA as compared with a leakage current of several nanoamperes in non-trench isolated switches.

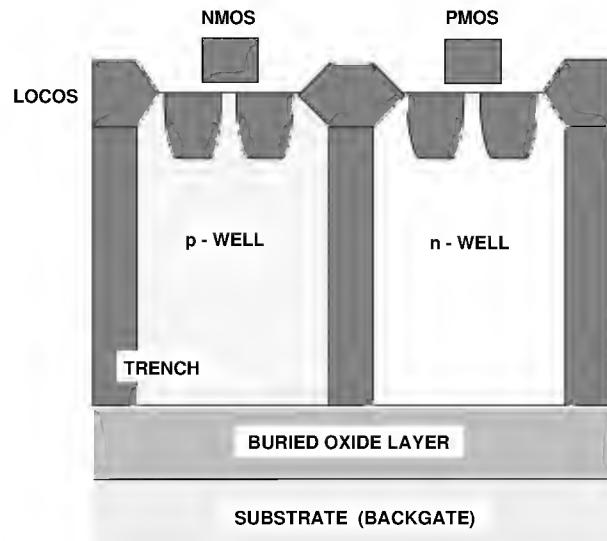


Figure 1. Trench Isolation

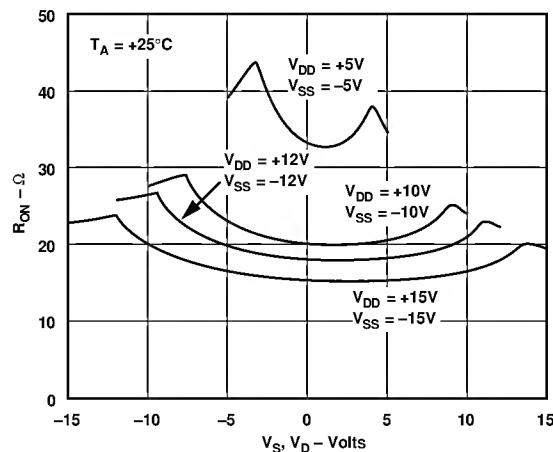
Typical Performance Graphs

Figure 2. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

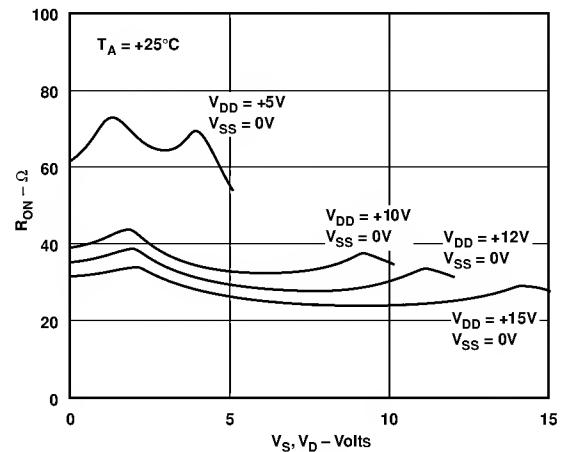
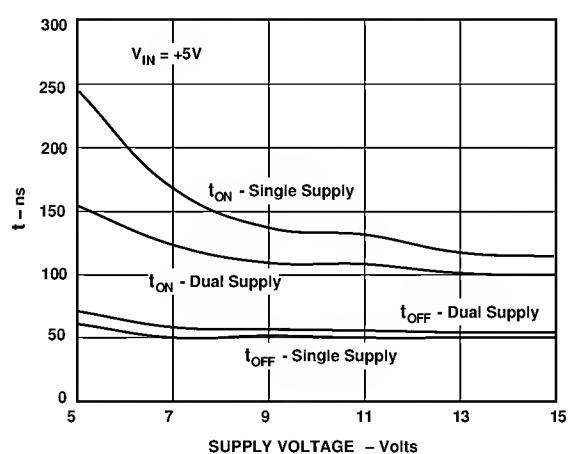
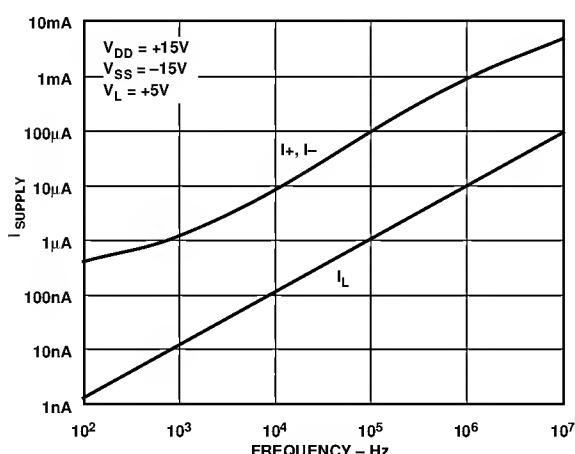
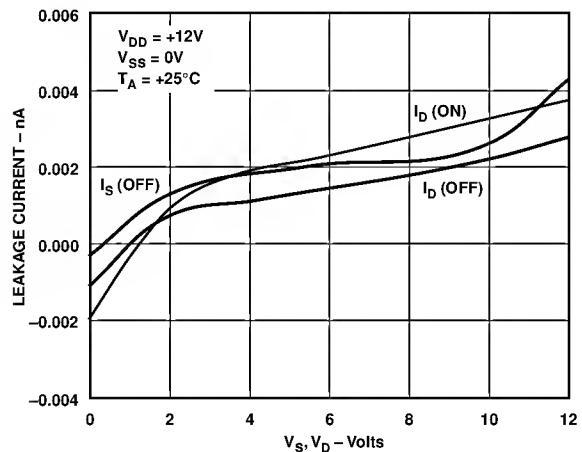
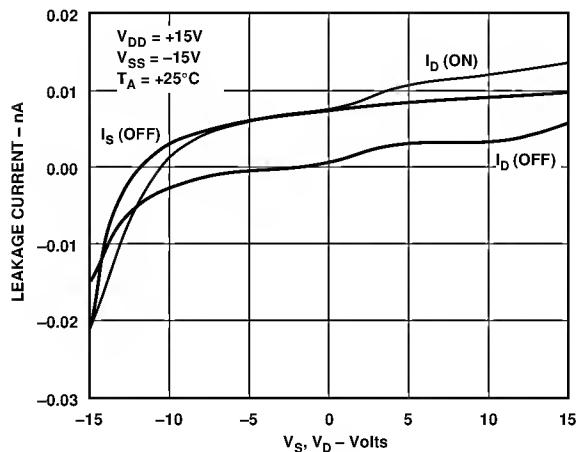
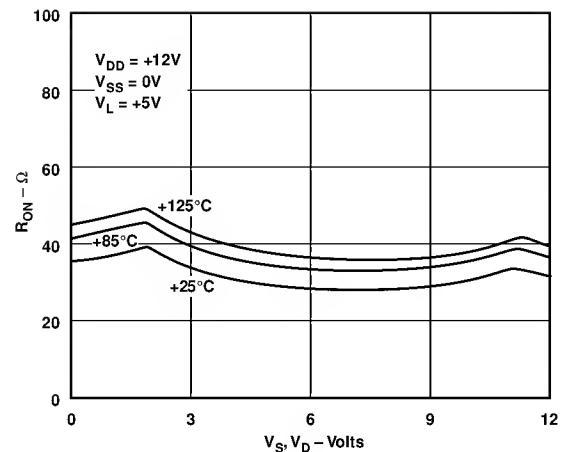
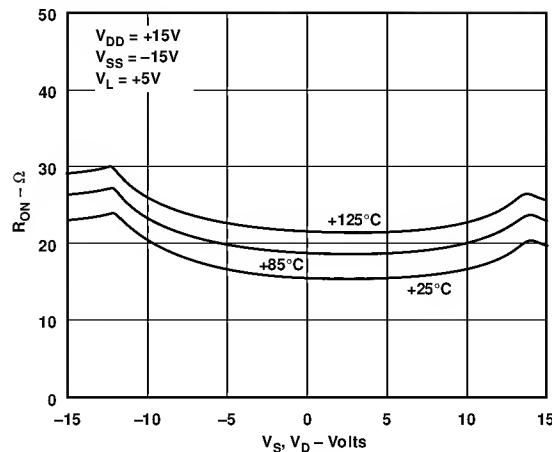
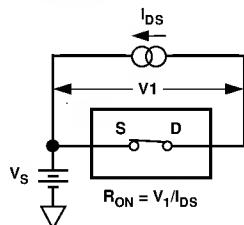


Figure 3. R_{ON} as a Function of V_D (V_S): Single Supply Voltage

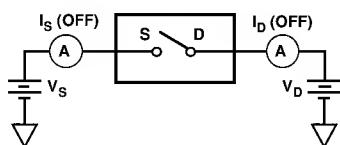
Typical Performance Graphs



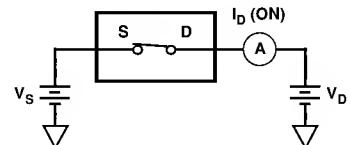
Test Circuits



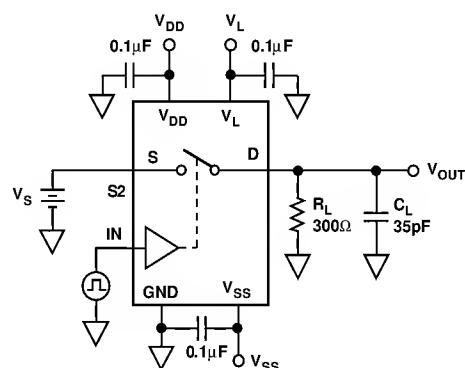
Test Circuit 1. On Resistance



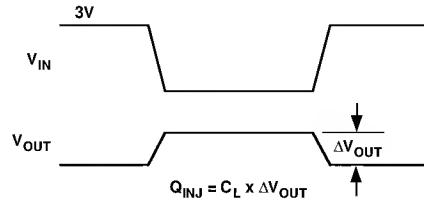
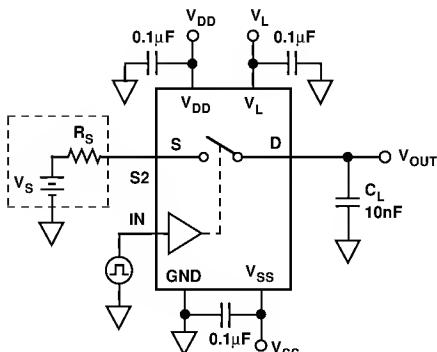
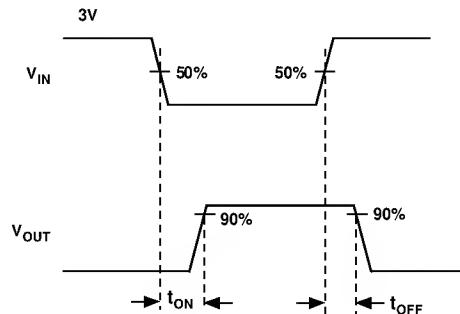
Test Circuit 2. Off Leakage



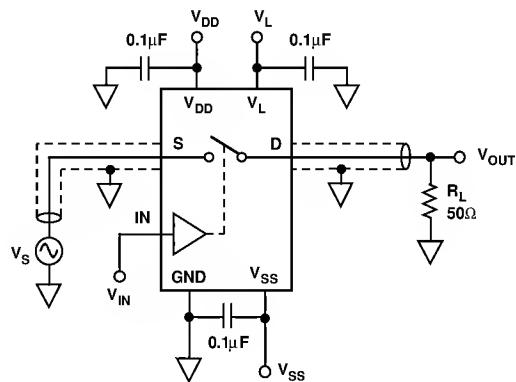
Test Circuit 3. On Leakage



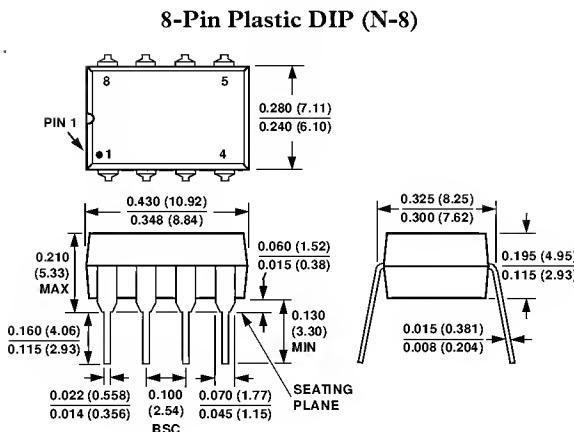
Test Circuit 4. Switching Times



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).**8-Pin SOIC (SO-8)
(Narrow Body)**